** San Francisco Bay University**

**EE461 Digital Design and HDL**

**Week#4 Combinational Logic (continue)**

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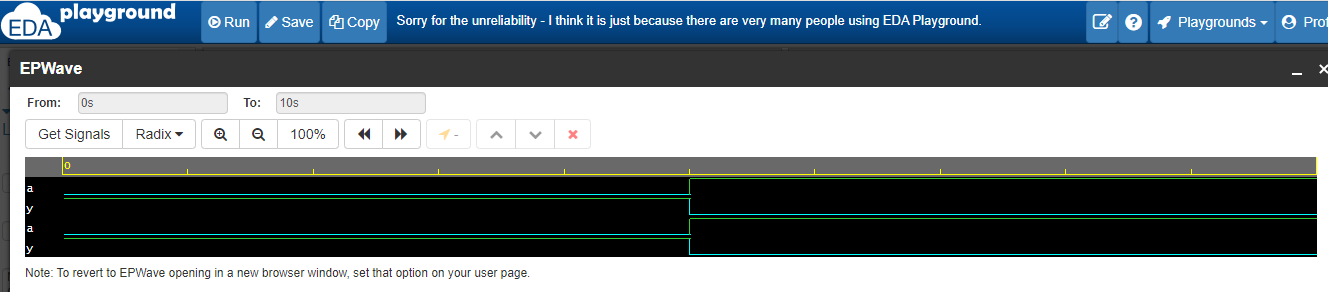
**1. Lab Outlines:**

1. Continuous assignment in combinational logic
2. Combinational logic in "always" block
3. Exercises

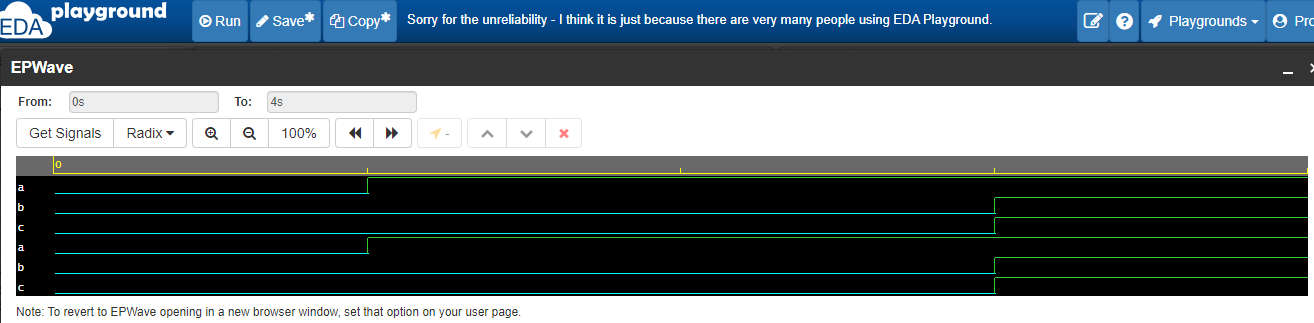
**2. Lab Procedures**

**I. Exercises**

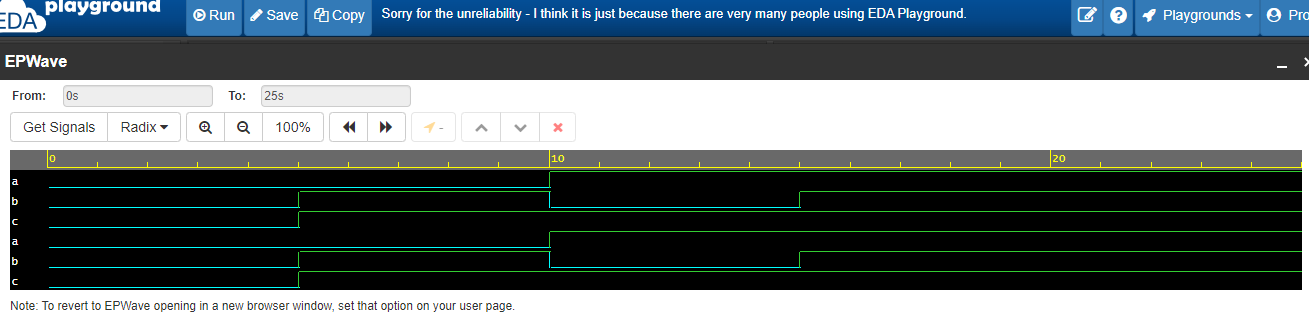
1. Design the following 2-bits RTL level combinational logic modules in continuous assignment and always blocks for each gate and write the testbench to verify your design covering all the test case by showing the waveforms,
   1. 1-bit NOT gate



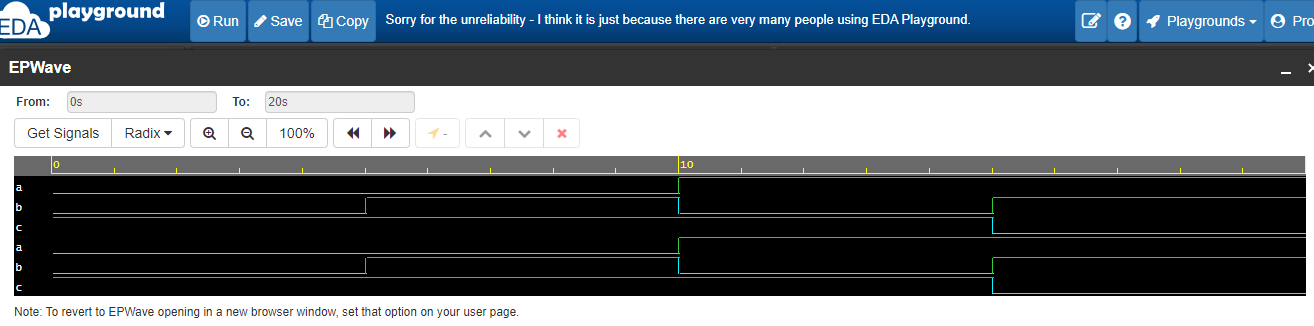
* 1. 2-bits AND gate



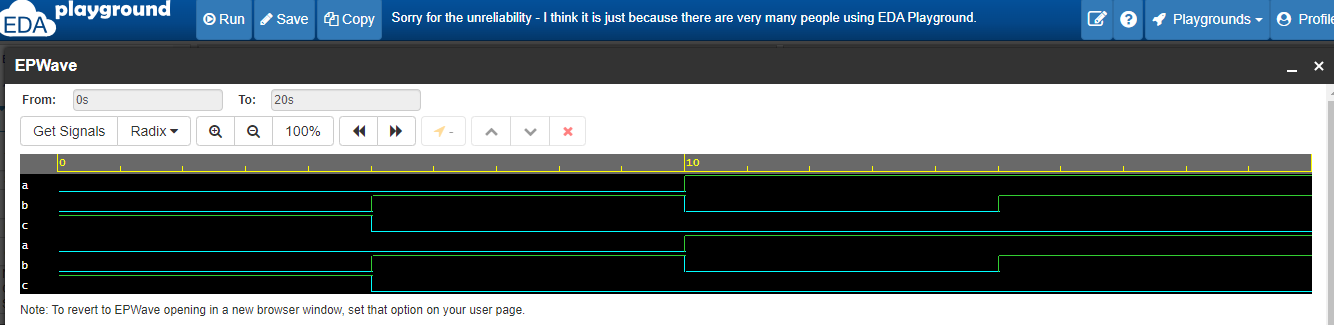
* 1. 2-bits OR gate



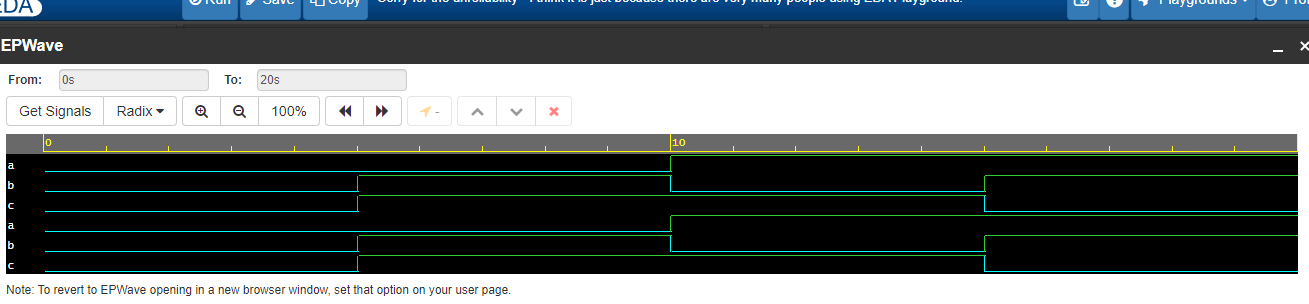
* 1. 2-bits NAND gate



* 1. 2-bits NOR gate



* 1. 2-bits XOR gate



* 1. 2-bits XNOR gateS

